MONOLITHIC BROADBAND POWER AMPLIFIER AT X-BAND

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ABSTRACT

Single-ended broadband power amplifier for X-band operation was designed and fabricated on GaAs with chip dimensions of 4.3 x 2.1 x 0.1 mm. The amplifier exhibited over 2 GHz of 1 db small signal bandwidth with more than 1.6 W at 9 db gain at mid-band CW operation with 20% power added effieicnty. The recently developed, potentially high yielding, Ta_2O_5 capacitor technology enabled the small chip size.

CHIP DESCRIPTION

We have fabricated a single-ended cascaded two-stage power amplifier for X-band broadband operation on GaAs. The chip dimensions are 4.3 x 2.1 x .1 mm. The FET devices have total peripheries of 2 mm and 4 mm with unit gate width of 200μm. The nominal gate to gate and source to drain separations are respectively 30μm and 6.8μm. A photo of a chip is shown in Fig. 1.

The 1μm gate is recessed with a contact N^+ layer .3μm thick doped to 2×10^{18} ions/cm^3 reaching to the edge of the narrow recess. The active channels are processed in an epi layer .4 μm thick doped to 9×10^{16} ions/cm^3 grown on a buffer layer 1.6μm thick on semi-insulating Cr-doped GaAs substrate. The individual source fingers are connected by air bridges which are raised 2.5μm above a .5μm thick polyimide passivating film. Via holes are used to ground the two ends of the sources as well as the bypass capacitors. The gate metallization is Ti/Pt/Au while the transmission lines are Au plated to a nominal thickness of 3μm.

The amplifier is designed to allow power-combining of up to four units. To this end it is symmetric along its input/output axis; DC biases can be applied from either side. Separate gate and drain bias pads are provided to each stage. Three Si_3N_4 decoupling/matching capacitors of values 1.55, .63 and 1.36 pF are provided in the input, interstage and output matching networks. Eight bypassing Ta_2O_5 capacitors, 50 pF each, are also provided.

POWER AMPLIFIER DESIGN

The unique feature of a power amplifier, in contrast to a small signal amplifier, is the non-linear behavior of the active FET devices. Both the input and output loads required for optimum power match are nonlinear functions of drive level. Two basic approaches to the design problem are possible.

One straightforward approach is to measure the output load presented to the FET as a function of the power delivered to the load. This is the load-pull method. Its main disadvantages are two: first, the measurements are tedious with inherently low accuracy, and second and most important, the method is very difficult to implement for the design of a broadband multistage power amplifier. Since no analytical model is associated with the load-pull measurements, analytical performance analysis, needed for design with actual non-unilateral FETs with fabrication tolerances and variations, is extremely difficult.

The second approach which we have adopted, is to develop a large signal, physically rooted model of the FET devices and use analytical methods to design the two-stage amplifier. The model which we used is the one presented by A. Platzker and Y. Tajima[1] which in turn is an extension of an earlier model by Y. Tajima et al[2]. The model which is described by a set number of parameters, is based on small signal S-parameter measurements, DC I-V curves and the physics of the FET devices. An in-house CAD program, LSFET, was developed to analytically calculate the power performance of discrete FET devices as well as multi-stage (up to two stages) power amplifiers as a function of power. This program as well as the commercially available COMPACT program, were used extensively in our design.

The steps which we follow in designing two-stage power amplifiers begin with the output and progress toward the input. Upon selecting the periphery of the output FET, in accordance with its capability to deliver the required power, its optimum output impedance is determined by LSFET.

In the next step, the output matching stage is designed. The function of any of the three matching networks, input, interstage and output is to match the output impedance which terminates it, to the required input impedance while at the same time allowing for the introduction of the proper DC biases. This dual function should be performed with minimum interference, i.e. with maximum isolation between the RF and DC circuitry. The cut off frequency should be low enough to suppress the natural tendency of circuits with even medium periphery devices to oscillate at far out of band low frequencies. In the case of the output matching

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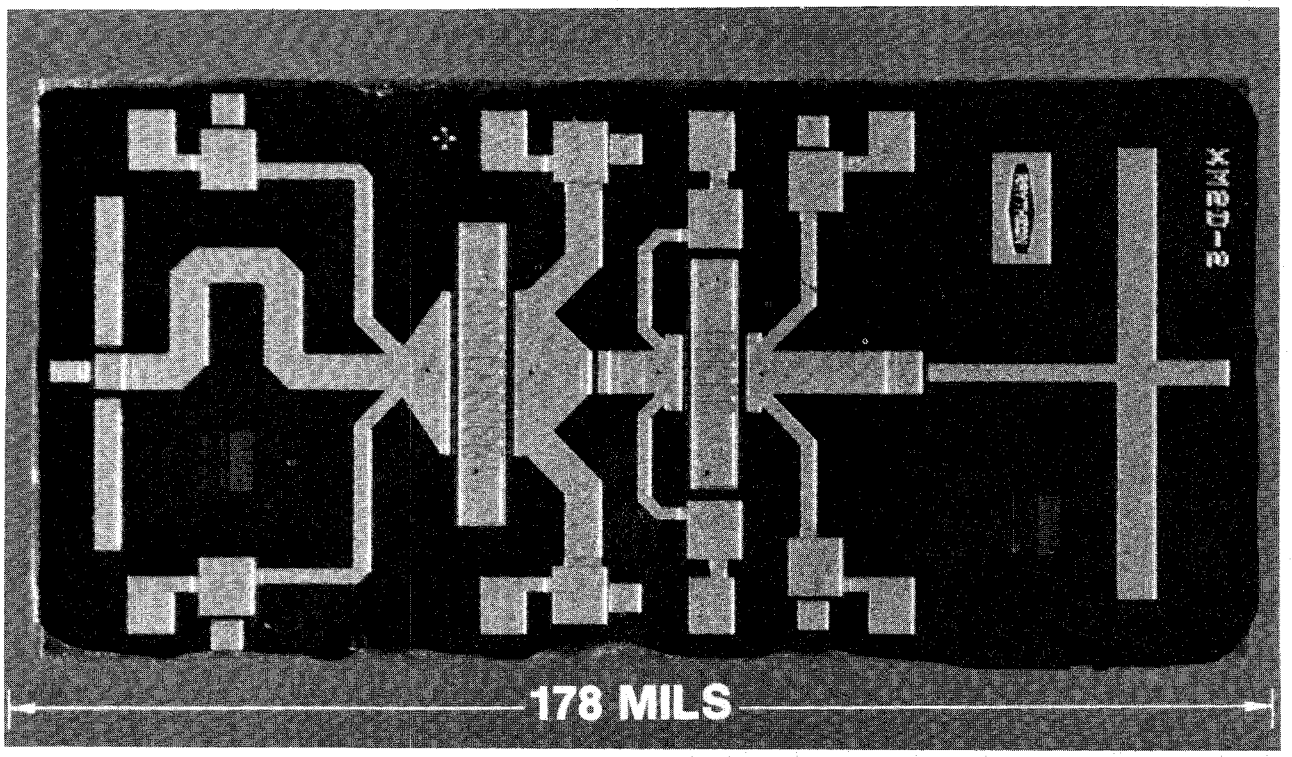

Fig. 1. Photograph of X-band power amplifier chip.

network, it should be designed to present to the output FET the optimum impedance it requires while the network is terminated with 50Ω. This step is best performed by a program such as COMPACT. Once a circuit with realizable element values is obtained, we proceed to the next design step which is the determination of the required input impedance to be presented to the output FET. This is done again with LSFET.

The next few steps are a repitition of the previously described ones but with respect to the driver FET in the first amplifier stage.

The last step in the amplifier design is the determination of the input matching network. This is done by optimizing the overall small signal performance and input match of the amplifier. During this last step, the interstage and output elements are naturally kept constant. A final verification of the power performance of the circuit is done with LSFET.

In selecting the topology of any of the matching networks, proper attention should be given to the special constraints presented by the MMIC technology. In particular, line impedances are limited to the range of 20-80Ω and capacitor values cannot be produced with tolerances of less than $\pm$ 15% over a large wafer. Two particular requirements arise in the case of large periphery devices. DC current carrying lines should be capable of handling the maximum allowable mil spec current density of .5 Mega Amp/cm^2 and large bypass capacitors on the gates and drains should be used. In our case we used Ta_2O_5 dielectric capacitors whose specific capacity is 10 times larger than the commonly used Si_3N_4 capacitors. Their availability enabled us the usage of 50 pF bypass capacitors which insured negligible bias interference. The minimum acceptable values for adequately bypassing the 4 mm periphery devices were found to be 30 pF.

For decoupling purposes, however, Ta_2O_5 capacitors cannot be used since by the very nature of their high capacity, their minimum practical value is 10 pF. Where smaller values were needed, Si_3N_4 capacitors were used. In our circuit, we used three Nitride decoupling capacitors and eight Tantalum bypassing ones. The details of the Tantalum process were given by M. Durschlag and J. Vorhaus[3].

AMPLIFIER PERFORMANCE

The amplifier was designed to operate over the 8.5 - 10.5 GHz range. The small signal performance was measured over the range of 6-12 GHz while the power performance was measured over the 8.5 - 11 GHz range. The measured power performance at small signal and at the 1 db compression points are presented in Fig. 2. The maximum power of 32.1 dbm at 9 db gain was obtained at 9 GHz tapering to 31.5 db at 8.5 GHz and 9.5 GHz with the same gain. The 1 db compression at 10 GHz was at 30.4 dbm with a gain of 7 db. At 6 db gain, 31.3 dbm were achieved at 10 GHz. All the numbers quoted above pertain to an assembled amplifier unit with jig losses estimated conservatively at 1 db not subtracted. The actual chip performance should be increased by 1 db in gain and 1/2 db in power. The

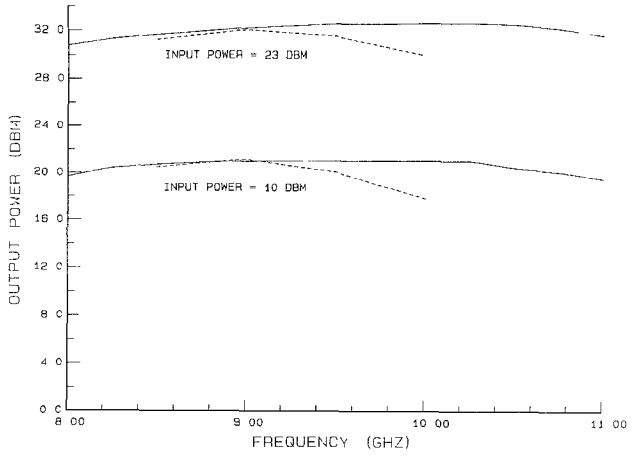

Fig. 2. Small signal and power performance. Solid line - original design, dashed-measurement.

power added efficiency of the CW performance was 20% with drain biases of ~8.5 V and a total DC current of 800 mA.

The small signal performance is shown in Fig. 3. As can be seen in the figure, the small signal 1 db

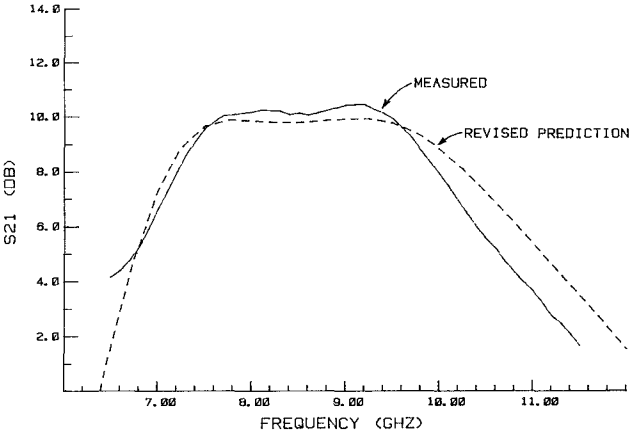

Fig. 3. Small signal performance.

bandwidth is over 2 GHz with a gain of 10 db. It can also be seen from Figs. 2 and 3 that the performance is shifted downwards in frequency with the operating band somewhat smaller than originally designed.

Several causes contributed to the observed deviation in the amplifier performance. The combined effect of these causes led to the revised performance perdiction shown in Fig. 3. The excellent agreement between it and the observed performance is an object lesson in the power and importance of computer analysis in MMIC design.

The amplifier was originally designed with non-passivated devices which were characterized and modelled. When test devices, processed on the same wafers as the amplifiers, were analyzed, it was found that their element values changed somewhat with the main difference, as anticipated, in the values of S12, specifically, the magnitude increased by roughly a factor of two. No agreement, however, was obtained when the new FET models were used in the circuit. Increasing the values of the Si_3N_4 capacitors by roughly 40% contributed towards closing the gap between prediction and observation. In subsequent measurements we were able to determine that a subtle unforeseen new processing step was indeed responsible for this increase in the coupling capacitors -- an increase well outside the tolerances allowed for the variation in these components. A third contributor was the fact that the wafers were erroneously thinned to 75μm instead of 100μm. A final contributor was the test jig. With all four contributions, the revised performance prediction is seen to be, as already stated, in excellent agreement with the actual observation.

CONCLUSIONS

We have demonstrated the feasibility of processing broadband single-ended high power monolithic amplifiers for X-band operation with high power added efficiency. The sources of deviations of performance between predictions and acutal observation were identified and corrective steps were being taken to eliminate them in future circuits.

REFERENCES

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